UTILITY PATENT APPLICATION TRANSMITTAL

☐ DUPLICATE

Address to:	Attorney Docket No.	EM/LEE/5990
Assistant Commissioner for Patents Box PATENT APPLICATION Washington, DC 20231	First Named Inventor (or identifier)	Young Su LEE
	Total Pages	61

Transmitted herewith is a patent application under 37 CFR 1.53(b).

Entitled: MOTION ESTIMATOR ARCHITECTURE FOR LOW BIT RATE IMAGE COMMUNICATION

☒ 1. **Submitted herewith are the following:**

24 pages of specification, including claims and Abstract.
10 sheets of FORMAL drawings.
7 claims.
1 Oath/Declaration signed by each inventor.
1 signed Small Business Small Entity Statement.
1 certified copy of Korean appl no. 10-2000-42044, filed July 21, 2000. Priority is claimed.
1 Assignment of the invention, Cover Sheet, and payment of the $40.00 recordal fee.
1 check in the amount of $385.00 including any assignment recordal fee.

☒ 2. **The Commissioner is authorized to credit any overpayment and charge any deficiency in any fees required under 37 CFR 1.16 and/or 1.17, to Deposit Account No. 02-0200.**

☐ 3. Insert before the first sentence of the specification: - - This application claims the benefit of provisional application number _____ filed _____. - -

☐ 4. Insert before the first sentence of the specification: - - This application is a Continuation-in-part of nonprovisional application number _____ filed _____. - -

☐ 5. Other:_____.

THE FILING FEE IS CALCULATED AS FOLLOWS:				Basic Fee:	$690.00
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Independent Claims:	1	- 3 =	0	X $78 =	0.00
Correspondence Address: BACON & THOMAS, PLLC 625 Slaters Lane, 4th Floor Alexandria, VA 22314-1176				Multiple Dependent Claim (add $260.00):	0.00
				Subtotal:	690.00
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Date:	Name:	Signature:	Reg. No.
September 8, 2000	Eugene Mar		25,893

Small Business

VERIFIED STATEMENT (DECLARATION) BY A SMALL BUSINESS CLAIMING SMALL ENTITY STATUS UNDER *37 CFR 1.9(F) AND 1.27(C)*

Applicant or Patentee: LEE, YOUNG SU
Docket #:
Serial or Patent Number:
Group Art Unit:
Filed or Issued:
Examiner:
Title: MOTION ESTIMATOR ARCHITECTURE FOR LOW BIT RATE IMAGE COMMUNICATION

I hereby declare that I am

- ☒ the owner of the small business concern identified below:
- ☐ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Concern: C&S TECHNOLOGY CO., LTD.
Address: HAEJOO BUILDING, NONHYUN-DONG, 175-4, KANGNAM-GU, SEOUL, 135-010, KOREA

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in *13 CFR 121.3-18*, and reproduced in *37 CFR 1.9(d)*, for purposes of paying reduced fees under *section 41(a) and (b) of Title 35, United States Code*, in that the number of employees of the concern, including those of its affiliates, **does not exceed 500 persons**. For purposes of this statement, (1) the number of employees is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

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- ☐ The patent application identified above.
- ☐ The PCT International patent application identified above.
- ☐ The patent number identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention must file separate verified statements averring to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under *37 CFR 1.9(c)* if that person made the invention, or by any concern who would not qualify as a small business concern under *37 CFR 1.9(d)*, or a nonprofit organization under *37 CFR 1.9(e)*. Each person or organization having any rights in the invention is listed below:

- ☒ no such person, concern or organization.
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I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate *(37 CFR 1.28(b))*.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine, or imprisonment, or both, under *section 1001 of Title 18 of the United States Code*, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which the verified statement is directed.

Name and Title SEO, SEUNG MO· C&S TECHNOLOGY CO., LTD.	*Date* SEPTEMBER 4, 2000
Address HAEJOO BUILDING, NONHYUN-DONG, 175-4, KANGNAM-GU, SEOUL, 135-010, KOREA	*Signature*

MOTION ESTIMATOR ARCHITECTURE FOR LOW BIT RATE IMAGE COMMUNICATIOIN

BACKGROUND OF THE INVENTION

1. Technical field

The present invention relates to an adaptable motion estimator architecture for low bit rate image communication. Particularly, the present invention relates to a technique to implement a motion estimator which has a reduced size of hardware and is compatible with characteristics and a bit rate of an applied image.

2. Description of the Prior Art

Generally, an image data compression/decompression technique is an essential one used in various fields such as multimedia communication, broadcast, storing media, etc. There are several standards for the image data compression/decompression such as JPEG (Joint Photographic Experts Group), MPEG (Moving Picture Experts Group), H.261/H.263, etc. Among them, H.261/H.263 is broadly used for low bit rate image communication.

Particularly, there are two methods of compressing the moving pictures: spatial compression and time compression. The spatial compression mainly employs DCT (Discrete Cosine Transform), Huffman Coding, DPCM (Differential Pulse Code Modulation), RLC (Run

Length Coding), and so on. The time compression mainly uses Motion Estimation.

The motion estimation enhances the bit rate by obtaining a moving vector corresponding to a position with the least difference in a given search area of a previous frame to send a 16×16 macro block of a current frame by using a time relation between the previous frame and the current frame. The motion estimation is used in all encoders to which MPEG and H.261/H.263 standards are applied.

FIG. 1 is a schematic view for illustrating concept of a macro block in the current frame.

As shown in FIG. 1, a size of the macro block in the current frame is indicated in 16 pixels × 16 pixels by the MPEG and H.261/H.263 standards and defined as a macro block 10.

In case of a CIF (Common Interchange Format) having a current frame size of 352 pixels × 288 pixels, 396 macro blocks 10 exists in each frame and 396 times of motion estimations are needed.

In case of 1/4 CIF (Quarter CIF; hereinafter referred as QCIF) having a current frame size of 176 pixels × 144 pixels, it can be understood that 99 times of motion estimations are needed in one frame.

FIG. 2 is a schematic view for illustrating concept of a search window and a motion vector.

As shown in FIG. 2, the current macro block 10 in a current frame moves in a pixel unit on a search area of a previous frame and finds a macro block having a least difference.

At this time, a position of the current macro block 10 and a position of a best match block 20 are indicated as a motion vector 30 on the previous frame.

Computational complexity and memory bandwidth of the motion estimator may estimate motion as shown in FIG. 2 when using a full search method, which is a representative motion estimating method.

Of course, provided that a size of the macro block is 16 pixels × 16 pixels and a distance of the search window is 8, the numbers of available vectors are –8 ~ +8 at X-axis and –8 ~ +8 at Y-axis. Also, 289 times of comparisons are required for 17 pixel × 17 pixel macro blocks.

In order to find out the most similar macro block 10 among the 289 motion vectors, MAE (Mean Absolute Error) is mainly used and a value corresponding to a least MAE is determined as the motion vector 30.

MAE is obtained by adding an absolute value of a difference between a current pixel and a previous pixel, which is identical to a value adding an absolute value of a 16 pixel × 16 pixel difference.

In other word, because there are all 99 macro blocks in QCIF and MAE requires 289 calculations for each block, about 99×289 (28,611)

times of MAE calculations are needed in one frame.

In fact, MAE calculations are performed less than 28,611 times. Because the search area is limited for macro blocks in a frame boundary, 23,427 times of macro block comparisons are needed in consideration of the boundary.

Such motion estimation requires much computational complexity and very large memory bandwidth, which make it difficult to implement such technique into hardware.

The previous frame data and the current frame data are generally stored in DRAM (Dynamic Random Access Memory). The reason is that there is quite a large amount of the frame data. For example, about one MEGA bit memory is required to store one frame of CIF.

In addition, in order to access a comparison macro block data of the previous frame from DRAM whenever comparing the macro blocks, a very large memory bandwidth is needed.

As shown in FIG. 2, in case of QCIF, an image format and a moving picture of 15 frames per second, 23,427×16×16×15 bytes/second (about 90 Mbytes/second) of memory bandwidth is required. Due to such big memory access, a high speed SRAM (Static RAM) is usually used as a cache memory.

FIG. 3 shows a half-pixel position and its formula among the moving vectors of FIG. 2.

As shown in FIG. 3, capital letter A, B, C and D points indicate integer-pixel positions, while small letter a, b, c and d points indicate half-pixel positions. In the figure, it can be seen that there exist integer-pixel vectors and half-pixel vectors in the motion vector.

Formula 1

$$a = A$$

$$b = (A + B + 1) / 2$$

$$c = (A + C + 1) / 2$$

$$d = (A + B + C + D + 2) / 2$$

Therefore, motion of the half-pixel position can be estimated by the above Formula 1 using each of the integer-pixels and the half-pixels.

However, such conventional motion estimation has some problems described below.

First, the conventional motion estimation requires a large amount of computational complexity. Though a faster search algorithm such as a hierarchy search, a three step search, a sub-sampling search, etc. is announced to reduce the computational complexity, such search methods have difficulties in hardware applications. Therefore, the full search algorithm is mainly used.

Second, as a hardware structure for the full search, a systolic array is usually used. However, the systolic array has a drawback that it may increase a size of hardware and a load of synchronous clocks due to abundant registers for pipelines.

Third, in case of using the systolic array, a half-pixel function can be hardly included in an integer-pixel function. So, a separate hardware for the half-pixel function is needed.

SUMMARY OF THE INVENTION

Therefore, the present invention is designed to solve the problems of the prior art. An object of the present invention is to provide a motion estimation architecture for low bit rate image communication which may decrease a hardware size, and be compatible with image characteristic and bit rate.

Another object of the present invention is to provide a motion estimation architecture for low bit rate image communication which optimizes performance of the motion estimator by selectively applying a search method suitable for a low bit rate image characteristic and an encoder performance.

In order to accomplish the above object, the present invention provides a motion estimator architecture for low bit rate communication, which includes a previous frame storing unit for storing a previous

search window data of a current macro block from a previous frame memory. A current frame storing unit stores a current macro block data to find a motion vector in a current frame memory. A multiplexer multiplexes the previous search window data and the current macro block data to conform to data processing thereof. A data process unit having a plurality of processing elements calculates a mean absolute error (MAE) of the motion vector with the previous search window data and the current macro block data transmitted from the multiplexer. A comparing unit comparatively detects the MAE of each motion vector from the data process unt to detect a motion vector having a least MAE. A state controller controls data flows between the above components.

In another embodiment of the present invention, the motion estimator may estimate the motion vector using any of a full search method and an interlace search method according to image characteristics and a bit rate.

In another embodiment of the present invention, the motion estimator may estimate a final motion vector by searching –8 ~ +8 integer-pixels to X and Y-axes to obtain an integer-pixel motion vector and then searching 9 half-pixels including the integer-pixel motion vector.

In another embodiment of the present invention, the motion estimator may calculate a half-pixel motion vector by searching 9

integer-pixels and 3 half-pixels at the same time using 9 processing elements (PE) when searching the half-pixels.

In another embodiment of the present invention, the motion estimator may detect the motion vector by searching both integer-pixels and half-pixels at the same time.

In another embodiment of the present invention, the motion estimator may update data which is not overlapped with the previous search window data when bringing the search window data of the current macro block from the previous frame storing unit.

In another embodiment of the present invention, the motion estimator may calculate addresses differently depending on the fact that number of the update macro block is even or odd when estimating motion of the current macro block.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings, in which like components are referred to by like reference numerals. In the drawings:

FIG. 1 is a schematic view for illustrating concept of a macro block of a current frame;

FIG. 2 is a schematic view for illustrating concept of a search window of a previous frame and a motion vector;

FIG. 3 shows a position of a half-pixel vector of the motion vector in FIG. 2;

FIG. 4 is a block diagram for illustrating architecture of a motion estimator according to the present invention;

FIGs. 5a and 5b are for illustrating a half-pixel search process of the present invention;

FIGs. 6a and 6b are for illustrating a memory accessing method of the search window according to the present invention;

FIGs. 7a and 7b are for illustrating a full search method and an interlace search method according to the present invention;

FIG. 8 is a block diagram showing a configuration of first, second, third, fourth and fifth data processing elements (PE0~PE4) of FIG. 4 in detail;

FIG. 9 is a block diagram showing a configuration of a sixth data processing element PE5 of FIG. 4 in detail;

FIG. 10 is a block diagram showing seventh, eighth and ninth data processing elements PE6~PE8 of FIG. 4 in detail; and

FIG. 11 is a block diagram showing a configuration of a comparator of FIG. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

FIG. 4 is a block diagram for illustrating architecture of a motion estimator according to the present invention.

Referring to FIG. 4, the motion estimator includes a previous frame storing unit 100 for storing a previous search window data of a current macro block from a previous frame memory, a current frame storing unit 200 for storing a current macro block data to find a motion vector in a current frame memory, a multiplexer 300 for multiplexing the previous search window data and the current macro block data to conform to operation of each data processor, a data process unit 400 for calculating a mean absolute error (MAE) of the motion vector with the previous search window data and the current macro block data transmitted from the multiplexer 300, a comparator 500 for comparatively detecting the MAE of each motion vector from the data process unit 400 to detect a motion vector having a least MAE, and a state controller 600 for controlling data flows between the above components.

The motion estimation applied to the present invention is a method of compressing moving pictures by using a relation between moving picture frames. The method employs a technique to find a

movement degree of a certain block of the current frame on a search area of the previous frame and then encoding and sending a difference value between a pixel data and a motion vector having a least difference.

The previous frame storing unit 100 stores the search window data of the current macro block among the previous frame data, which has a memory size as suggested in Formula 2.

Formula 2

$$(PC_{mb} + (SD \times 2))^2 \times 8 \text{ bits}$$

where PC_{mb} is a macro block pixel count and SD is a search length.

In other word, if the search length is 8 in a 16 × 16 macro block, the memory size is $(16+(8 \times 2))^2 \times 8 = 1024 \times 8$ bits.

Therefore, in consideration of the motion estimation, a suitable output data width of the memory is 32 and the memory size can be inscribed as 256 × 32.

The current frame storing unit 200 stores the current macro block data to find the motion vector among the current frame data. A memory size of the current macro block is suggested in Formula 3.

Formula 3

$$\mathbf{PC_{mb}^2 \times 8\ bits}$$

where PC_{mb} is a macro block pixel count and 256 × 8 bits.

In other word, if the data width is 8, the memory size can be inscribed as 64 × 32 bit memory.

The data process unit 400 which calculates MAE of each motion vector with the previous frame data and the current frame data transmitted from the multiplexer 300 has 9 processing elements (PEs).

With use of the 9 processing elements, the data process unit 400 can calculate 9 motion vectors at the same time. There are three reasons that the data process unit 400 uses 9 PEs.

First, it may reduce a chip area. The systolic array needs 256 PEs, so requiring so big area. The 9 PEs are suitable for estimating motion of QCIF, mainly used for low bit rate image communication, as well as CIF.

Second, it ensures regular operation. If the search length is 8, there are 17 kinds of X-axis vectors in numbers of –8 to +8. There are also 9 X-axis vectors in right and left borders in numbers of –8 to 0, 0 to +8.

If using 8 PEs, the data process unit 400 may calculate 8 vectors at once. Therefore, in order to calculate 9 kinds of X-axis vectors in

numbers of –8 to 0, the data process unit 400 should perform operation for X-axis vectors in numbers of –8 to –1 first, and then another operation for 0.

Moreover, if calculating 17 kinds of vectors in numbers of –8 to 8 with the 9 PEs, the data process unit 400 calculates vectors in numbers of –8 to 0 first, and then in numbers of 0 to +8, so duplicating calculation for the number 0 vector. It ensures easy control and effective motion estimation.

Third, the 9 PEs ensure motion estimation of the half-pixel vector without any separate hardware.

In other word, 4 integer-pixel position points A, B, C, D are required to obtain a value of a half-pixel position (d) and the data process unit may calculate a value of the half-pixel with use of such points.

FIGs. 5a and 5b are for illustrating a half-pixel search method according to the present invention.

As shown in FIGs. 5a and 5b, processing elements (PE0 - PE4) calculate five half-pixels in X and Y-axes and PE5 calculate a half-pixel in Y-axis.

The calculated half-pixels are inputted to PE6 - PE8 to calculate the three half-pixels at the same time.

The half-pixel search method calculates vectors of neighbor nine

half-pixels including the motion vector obtained in an integer-pixel search. Because the data process unit may calculate three half-pixel vector with the 9 PEs, motion vectors of all half-pixels can be obtained with three calculations.

FIGs. 6a and 6b are for illustrating a memory access method of the search window according to the present invention.

As shown in FIGs. 6a and 6b, they show an efficient memory access method when bringing the previous image data in an external DRAM to memories of search windows 40a, 40b.

When estimating motion of the current macro block, the memory access method uses a phenomenon that the current macro block is overlapped with the search window 40b which the previous macro block has used among data to be brought to a memory of the search window 40a from the external DRAM.

In other words, when estimating motion of the macro blocks each time, the method does not bring all of the previous image data in all search area but brings new data, now overlapped with the previous data. Therefore, the method may solve an address control problem by differently calculating an address according to the fact that the macro block has an even number or an odd number.

In addition, such method may reduce access time related to the external DRAM. The motion estimator suggested by the present

invention is designed to select the full search or the interlace search according to image characteristics and encoder performance.

FIGs. 7a and 7b are for illustrating the full search and the interlace search according to the present invention.

FIGs. 7a and 7b respectively show the full search and the interlace search. The full search may calculate the most accurate motion vector because it calculates motion vectors in all search area.

However, because of performing the motion estimation for all vectors, the full search may deteriorate encoder performance due to increased computational complexity in case that a speed of the motion estimation determines a speed of the encoder.

Therefore, there is a need to increase proportion of encoding frames by efficient motion estimation suitable for the image characteristics. There is also a fast search algorithm to decrease computational complexity of the motion estimation. However, the fast search algorithm has disadvantages that it has difficulties to implement in hardware and it could not find as accurate motion vector as the full search.

The present invention performs the full search to find more accurate motion vector in case that the encoding frame proportion is low or in case of compressing a small image such as QCIF format, while performing the interlace search to find the motion vector rapid in case

that the encoding frame proportion is high and in case of compressing images bigger than CIF format.

A function of selecting the full search and the interlace search according to encoder performance is programmed. The reason of using the interlace search for rapid search is that the interlace search uses same hardware structure as the full search.

When enhancing accuracy of searching the motion vector, it is not preferable to use only the interlace search. In order to improve the search accuracy, the present invention calculates motion vectors with the interlace search first and then continues the searching operation by ±1 along Y-axis to calculate motion vectors again. Then, the present invention finally calculates motion vectors by searching 9 half-pixel vectors, so increasing accuracy.

FIGs. 8 to 10 show block diagram showing the first to ninth data processors, or processing elements (PE0 - PE8) of FIG. 4 in detail.

At first, the first to fifth processing elements (PE0 - PE4) shown in FIG. 8 includes four present processing elements (PPE0 - PPE4) 400a, 400b, 400c, 400d to which current pixel position data (CDATA) and previous pixel position data (PDATA) are transmitted through the multiplexer (MUX) by a Bit-rate Allocation Signal (BAS), a first adder (ADD1) 410, a scaler 420 and a second adder 430.

Because the first to fifth processing elements (PE0 - PE4) have 32

bits of memory bus width, 4 pixels can be brought at once from the memory. Therefore, each processing element (PE) is designed to calculate 4 pixels.

A basic operation of the processing elements (PE0 - PE4) is to calculate a pixel data difference of a present pixel position corresponding to a previous pixel position and then store the difference value in an accumulator.

Now, operations of the above components are described below in more detail.

The multiplexer (MUX) is classified into an integer-pixel and a half-pixel according to a half-pixel signal type. An output of MUX is PDAT – CDAT in case of the integer-pixel, while MUX outputs PDAT itself in case of the half-pixel. That is, in case of the half-pixel, MUX outputs PDAT, PDAT + 1, or zero.

It is because the half-pixel type determines the output of MUX. There are 4 types of half-pixels, which correspond to half-pixel position points a, b, c, d shown in FIG. 3.

For example, if the half-pixel type is the point a, the first present processing element (PPE0) 400a outputs only PDAT and the second to fourth present processing elements (PPE1 - PPE3) 400b, 400c, 400d output zero, so outputting a half-pixel value at the point a as a differential signal.

If the half-pixel type is the point d, PPE0 (400a) outputs PDAT + 1, PPE1 (400b) outputs PDAT1, and PPE2 (400d) outputs PDAT3, or PDAT +1. Such output values are added in the first adder (ADD1) 410 to output the half-pixel value through the scaler 420.

In addition, the MAE values calculated in PE when calculating the motion vector of the integer-pixel are compared in the comparator 500 to find a vector having the least MAE. The comparator 500 operates one time after determining MAE values of 9 vectors by control of the state controller 600.

On the other hand, the sixth to ninth processing elements (PE5, PE6 - PE8) shown in FIGs. 9 and 10 have similar structure to PE0 - PE4 shown in FIG. 8, and not described here in detail.

In the integer-pixel mode, the processing elements (PE5, PE6 - PE8) perform similar operations to PE0 - PE4. PE0 - PE4 are structurally different from PE5, PE6 - PE8 only in the half-pixel mode.

That is, in the half-pixel mode, PE0 - PE4 receive 4 pixels to make and send one half-pixel, and PE5 receives 4 pixels in Y-axis having integer-pixels in X-axis to make and send 4 half-pixels.

In addition, PE6 - PE8 receive the half-pixels from PE0 - PE5 and then calculates a difference from the current pixel data in a similar manner to the integer-pixel mode.

FIG. 11 is a block diagram showing a configuration of the

comparator of FIG. 4.

As shown in FIG. 11, the comparator includes a multiplexer (MUX) 510 for multiplexing 9 mean absolute errors (MAE0 - MAE8) inputted from the data process unit 400, a substrate module (SUB) 520 for selectively transmitting MAE inputted from the multiplexer 510, and a comparing unit 530 for comparing MAE from the substrate module 520 with a previous MAE (MAEP).

Operations of the comparing unit are described below in more detail.

At first, 9 mean absolute errors (MAE0 - MAE8) are selected according to a vector state one by one. The selected MAE is inputted into the substrate module 520, which subtracts a Zero Vector Weight (ZVW) in case of a zero vector.

The reason of subtracting ZVW in case of the zero vector is that it may increase encoding compression efficiency when the vector is 0. The comparing unit 530 compares MAE with MAEP. If MAE is less than MAEP, MAE is updated as MAEP. That is, a vector at that time is updated as the motion vector.

As described above, the motion estimator architecture for low bit rate image communication has various effects as below.

First, the present invention can be used in low bit rate image communication and is operable in a small memory bandwidth by

adopting a previous window memory and a current macro block memory. In addition, the present invention may reduce data access time from an external DRAM to the previous search window memory through a memory address control.

Second, the present may calculate motion vectors of an integer-pixel and a half-pixel with same hardware and improve performance with small hardware as a whole.

Third, the present invention may optimize performance of motion estimation by selectively applying a full search and an interlace search in accordance with image characteristics and encoder performance.

Fourth, the present invention can be applied to an image phone which requires high encoding efficiency due to small hardware and may be applied to all video encoders conforming to H.261/H.263 and MPEG.

The motion estimator architecture for low bit rate image communication according to the present invention has been described in detail. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

What is claimed is:

1. A motion estimator architecture for low bit rate communication comprising:

previous frame storing means for storing a previous search window data of a current macro block from a previous frame memory;

a current frame storing means for storing a current macro block data to find a motion vector in a current frame memory;

a multiplexer for multiplexing the previous search window data and the current macro block data to conform to data processing thereof;

data process means having a plurality of processing elements for calculating a mean absolute error (MAE) of the motion vector with the previous search window data and the current macro block data transmitted from the multiplexer;

comparing means for comparatively detecting the MAE of each motion vector from the data process means to detect a motion vector having a least MAE; and

state control means for controlling data flows between the above components.

2. The motion estimator architecture for low bit rate image communication as claimed in claim 1,

wherein the motion estimator estimates the motion vector using any of a full search method and an interlace search method according to image characteristics and a bit rate.

3. The motion estimator architecture for low bit rate image communication as claimed in claim 1;

wherein the motion estimator estimates a final motion vector by searching –8 ~ +8 integer-pixels to X and Y-axes to obtain an integer-pixel motion vector and then searching 9 half-pixels including the integer-pixel motion vector.

4. The motion estimator architecture for low bit rate image communication as claimed in claim 3,

wherein the motion estimator calculates a half-pixel motion vector by searching 9 integer-pixels and 3 half-pixels at the same time using 9 processing elements (PE) when searching the half-pixels.

5. The motion estimator architecture for low bit rate image communication as claimed in claim 3,

wherein the motion estimator detects the motion vector by searching both integer-pixels and half-pixels at the same time.

6. The motion estimator architecture for low bit rate image communication as claimed in claim 1,

wherein the motion estimator updates data which is not overlapped with the previous search window data when bringing the search window data of the current macro block from the previous frame storing means.

7. The motion estimator architecture for low bit rate image communication as claimed in claim 6,

wherein the motion estimator calculates addresses differently depending on that number of the update macro block is even or odd when estimating motion of the current macro block.

ABSTRACT

An adaptable motion estimator architecture for low bit rate image communication 1) to be compatible with image characteristic and bit rate with a reduced hardware size and 2) to optimize performance of the motion estimator by selectively applying a search method suitable for a low bit rate image characteristic and an encoder performance.

The motion estimator multiplexes a previous search window memory data from DRAM and a current macro block data for finding motion vectors to conform to each data processing elements (PE0 – PE8) and comparatively detecting MAE (Mean Absolute Error) of each motion vector with a previous frame data and a current frame data to find a motion vector having a least MAE.

The motion estimator may be applied to an image phone which requires high encoding efficiency due to small hardware and may be applied to all video encoders conforming to H.261/H.263 and MPEG.

FIG. 4

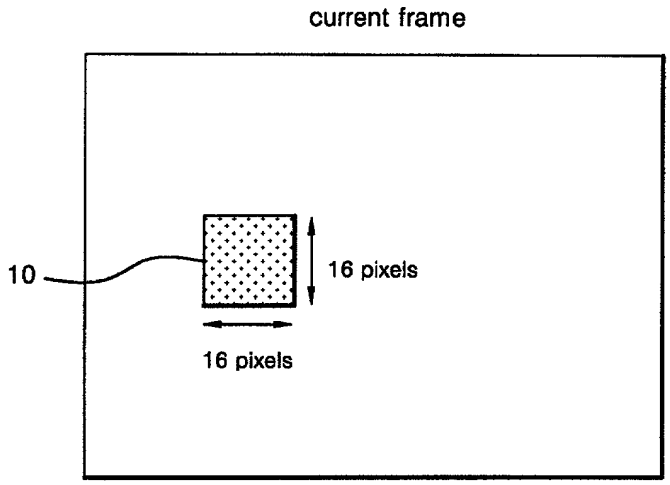
current frame
10
16 pixels
16 pixels

FIG. 1

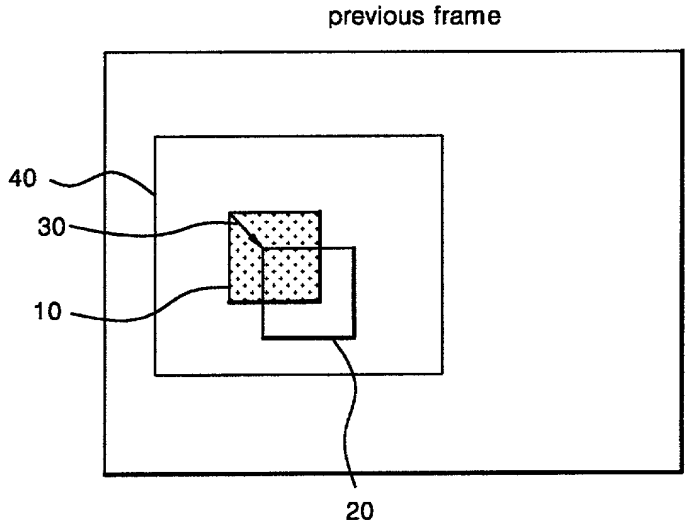
previous frame
40
30
10
20

FIG. 2

PRIOR ART

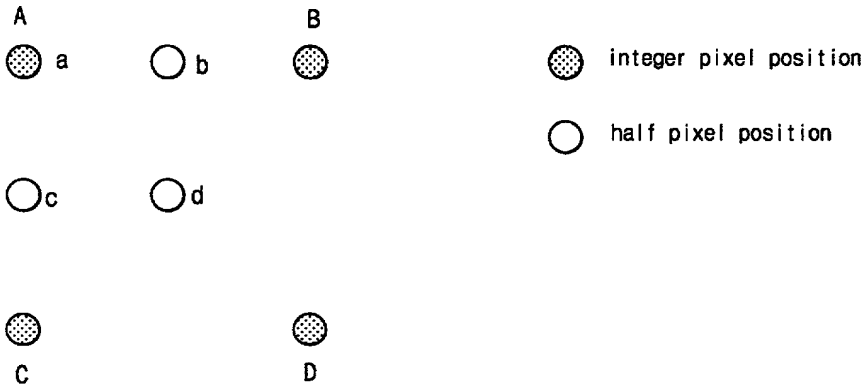

FIG. 3

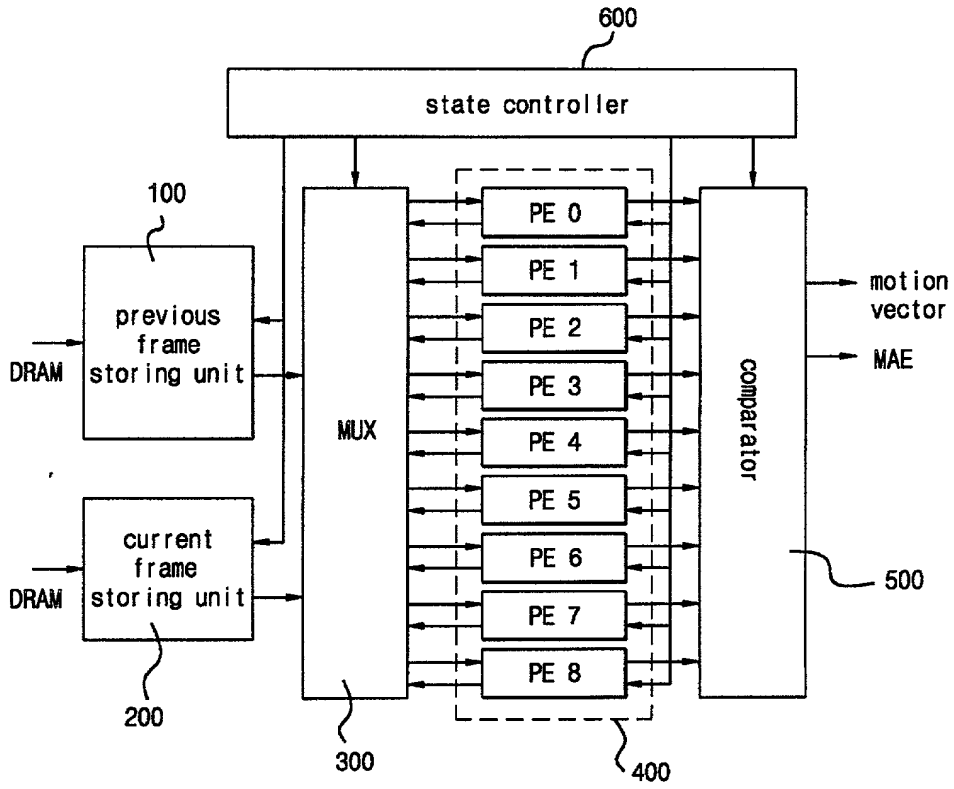
600
state controller
100
previous frame storing unit
DRAM
current frame storing unit
DRAM
200
MUX
300
PE 0
PE 1
PE 2
PE 3
PE 4
PE 5
PE 6
PE 7
PE 8
400
comparator
motion vector
MAE
500

FIG. 4

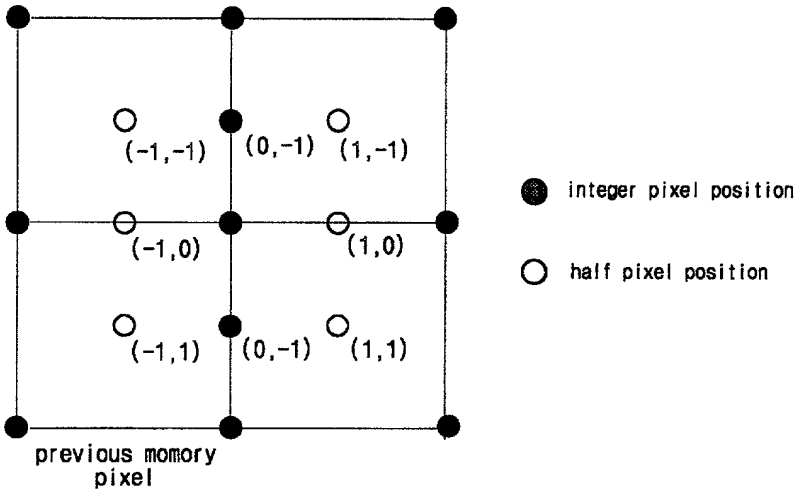
(-1,-1)
(0,-1)
(1,-1)
(-1,0)
(1,0)
(-1,1)
(0,-1)
(1,1)
previous momory pixel
integer pixel position
half pixel position

FIG. 5a

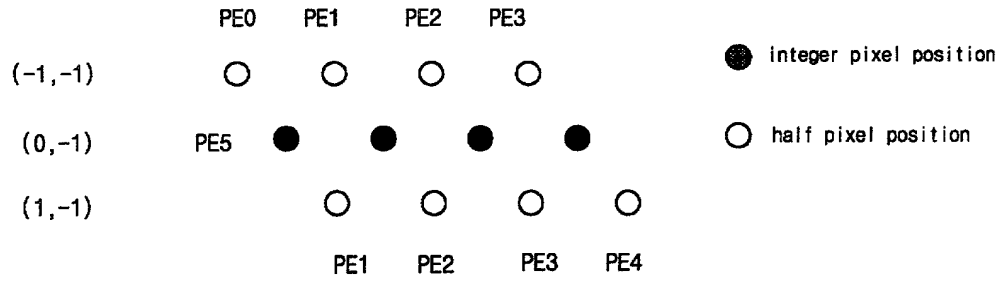
PE0
PE1
PE2
PE3
(-1,-1)
(0,-1)
PE5
(1,-1)
PE1
PE2
PE3
PE4
integer pixel position
half pixel position

FIG. 5b

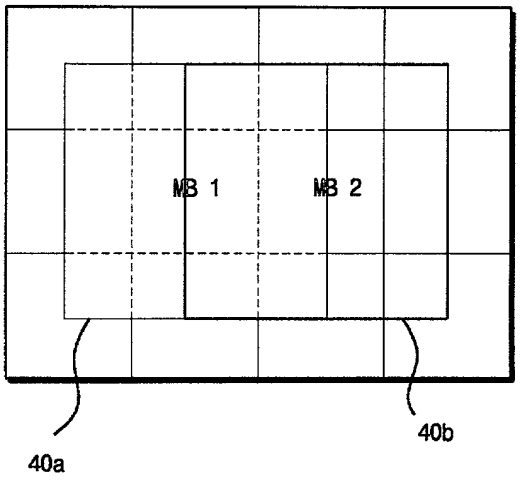

FIG. 6a

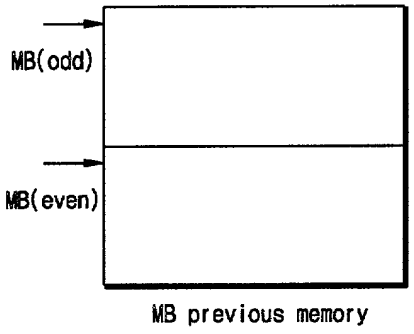

FIG. 6b

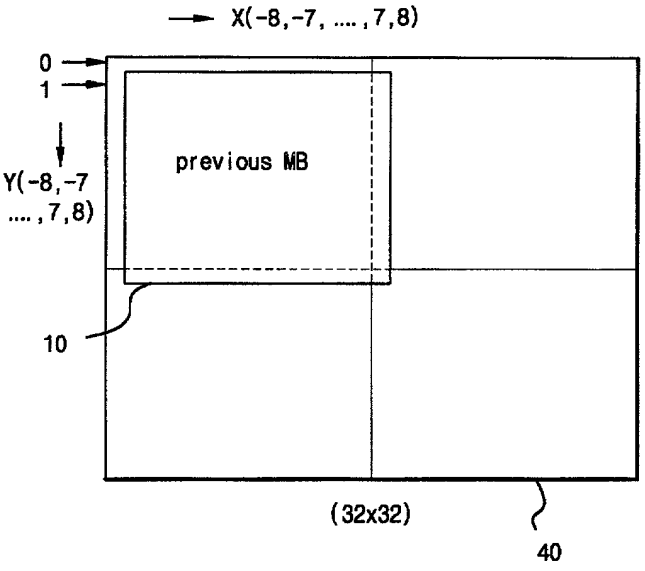
X(-8,-7, ... ,7,8)
0
1
Y(-8,-7
.... ,7,8)
previous MB
10
(32x32)
40

FIG. 7a

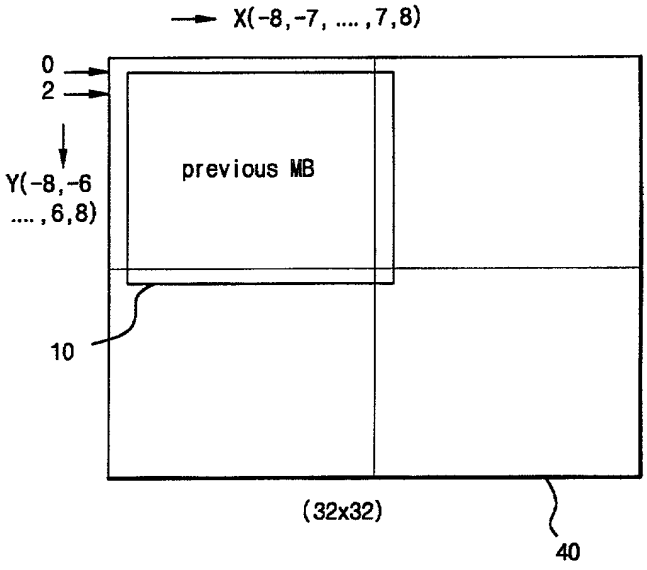
X(-8,-7, ... ,7,8)
0
2
Y(-8,-6
.... ,6,8)
previous MB
10
(32x32)
40

FIG. 7b

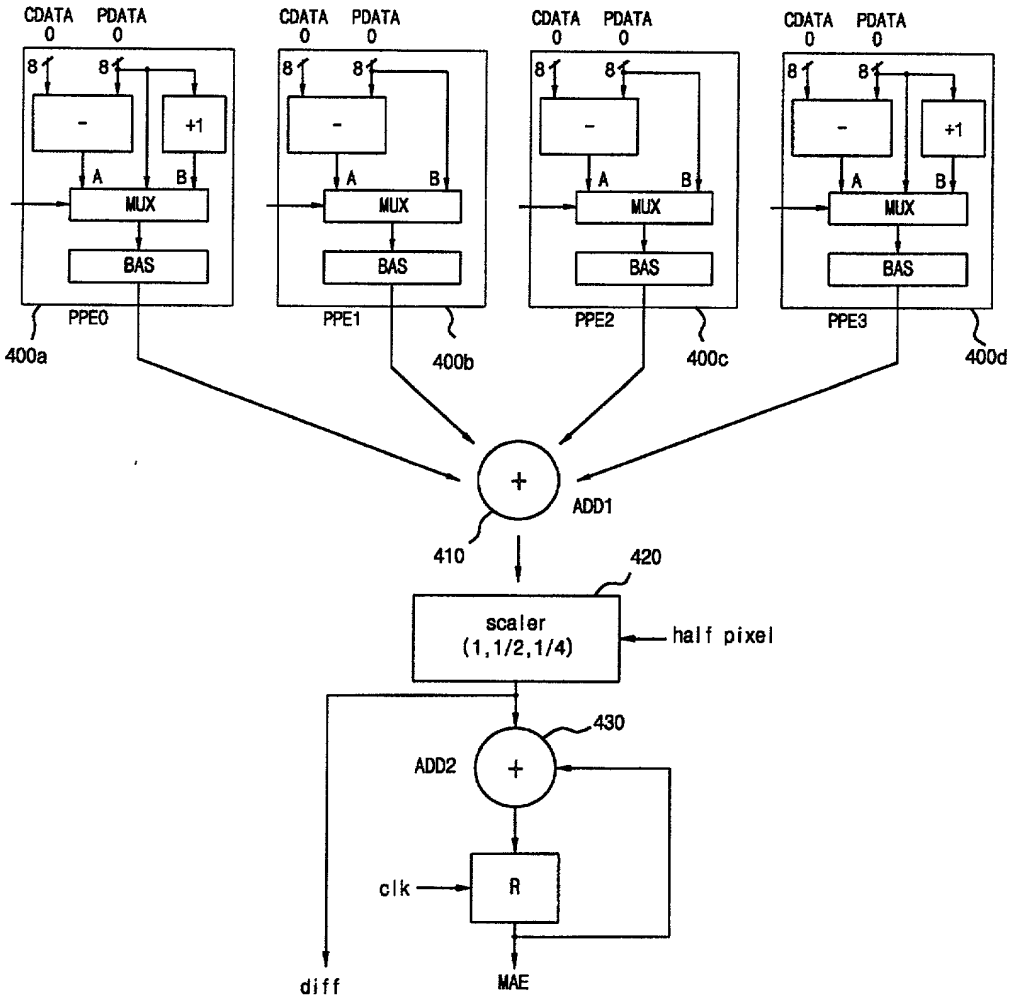
CDATA
PDATA
0
0
8
8
-
+1
A
B
MUX
BAS
PPE0
PPE1
PPE2
PPE3
400a
400b
400c
400d
+
ADD1
410
420
scaler
(1,1/2,1/4)
half pixel
430
ADD2
clk
R
diff
MAE

FIG. 8

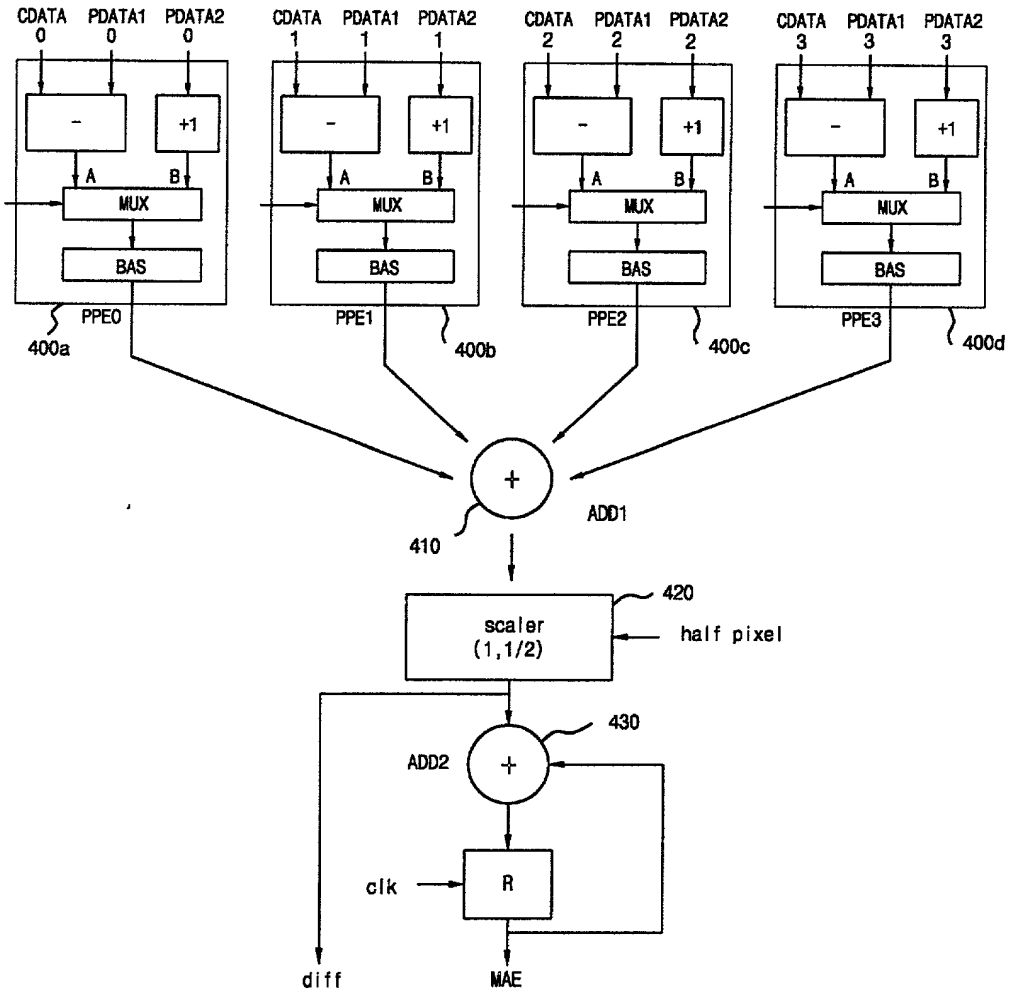
CDATA 0
PDATA1 0
PDATA2 0
CDATA 1
PDATA1 1
PDATA2 1
CDATA 2
PDATA1 2
PDATA2 2
CDATA 3
PDATA1 3
PDATA2 3
-
+1
A
B
MUX
BAS
PPE0
PPE1
PPE2
PPE3
400a
400b
400c
400d
+
ADD1
410
420
scaler
(1,1/2)
half pixel
430
ADD2
clk
R
diff
MAE

FIG. 9

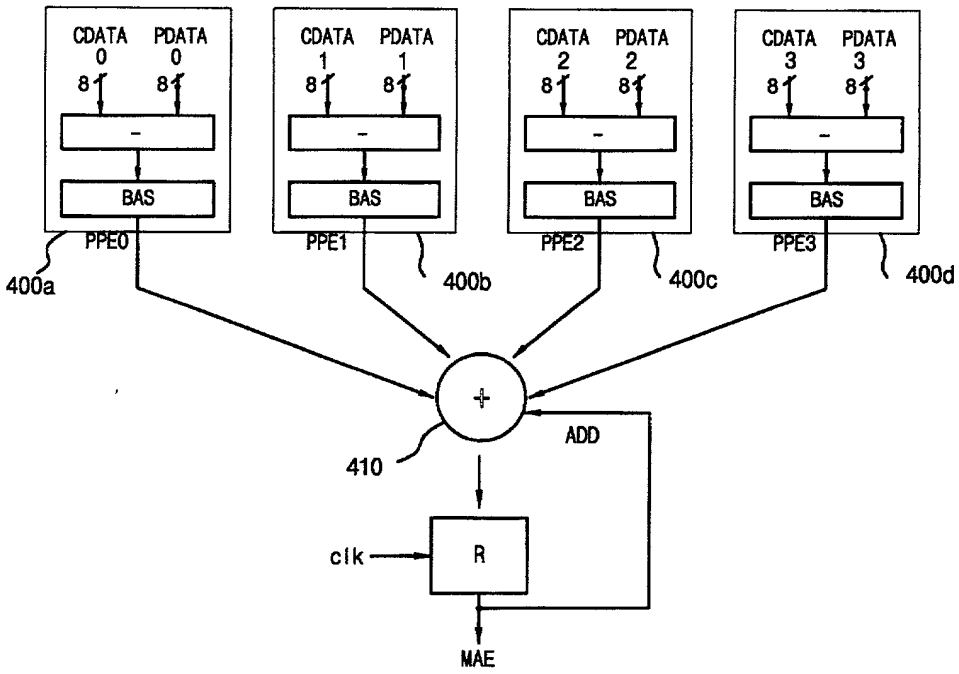
CDATA 0
PDATA 0
8
8
-
BAS
PPE0
400a
CDATA 1
PDATA 1
PPE1
400b
CDATA 2
PDATA 2
PPE2
400c
CDATA 3
PDATA 3
PPE3
400d
+
410
ADD
clk
R
MAE

FIG. 10

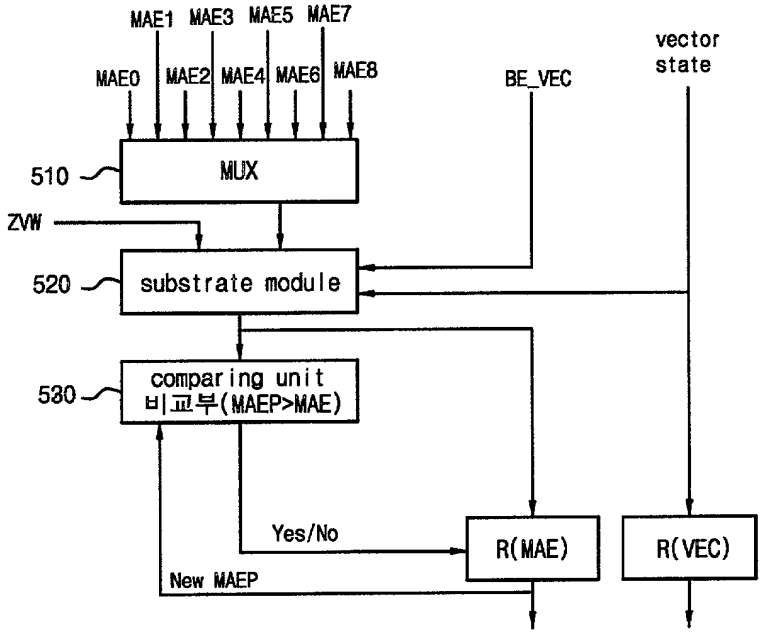
MAE1
MAE3
MAE5
MAE7
MAE0
MAE2
MAE4
MAE6
MAE8
BE_VEC
vector state
510
MUX
ZVW
520
substrate module
530
comparing unit
비교부(MAEP>MAE)
Yes/No
R(MAE)
R(VEC)
New MAEP

FIG. 11

ATTORNEY/DOCKET NO:

DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention (Design, if applicable) entitled:

MOTION ESTIMATOR ARCHITECTURE FOR LOW BIT RATE IMAGE COMMUNICATION

the specification of which (check one):

☒ is attached hereto, or ☐ was filed on: as U.S. Application Number or PCT International Application Number:

and (if applicable) was amended on:

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56*. I hereby claim foreign priority benefits under *Title 35, United States Code §119* of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	Country	Day/Month/Year Filed	Yes	No
10-2000-42044	KOREA	21/07/2000	X	

☐ Additional Priority Application(s) Listed on Following Page(s)

I HEREBY CLAIM THE BENEFIT UNDER TITLE 35 U.S. CODE §119(E) OF ANY U.S. PROVISIONAL APPLICATIONS LISTED BELOW.	
Application Number	Day/Month/Year Filed

☐ Additional Provisional Application(s) Listed on Following Page(s)

I hereby claim the benefit under *Title 35, United States Code, §120* of any United States application(s) or PCT international application(s) designating The United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of *Title 35, United States Code, §112*, I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56* which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	Filing Date	Status - Patented, Pending or Abandoned

☐ Additional US/PCT Priority Application(s) listed on Following Page(s)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under *section 1001 of title 18 of the United States Code* and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: I (We) hereby appoint as my (our) attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: J. Ernest Kenney, Reg. No. 19,179; Eugene Mar, Reg. No. 25,893; Richard E. Fichter, Reg. No. 26,382; Charles R. Wolfe, Jr., Reg. No. 28,680; Thomas J. Moore, Reg. No. 28,974; Bruce H. Troxell, Reg. No. 26,592; and

I(we) authorize my(our) attorneys to accept and follow instructions from _____ regarding any matter related to the preparation, examination, grant and maintenance of this application, any continuation, continuation-in-part or divisional based thereon, and any patent resulting therefrom, until I(we) or my(our) assigns withdraw this authorization in writing.

Send correspondence to: **BACON & THOMAS**
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FULL NAME OF FIRST OR SOLE INVENTOR	CITIZENSHIP
LEE, YOUNG SU	KOREA
RESIDENCE ADDRESS HAEJOO BUILDING 6F, NONHYUN-DONG, 175-4, KANGNAM-GU, SEOUL, 135-010, KOREA	POST OFFICE ADDRESS IS THE SAME AS RESIDENCE ADDRESS UNLESS OTHERWISE SHOWN BELOW
DATE SEPTEMBER 4, 2000	SIGNATURE

☐ *See following page(s) for additional joint inventors.*